## **ABSTRACT OF THE DISCLOSURE**

A computer-implemented method for identifying the best process path in a semiconductor manufacturing process for processing a plurality of wafer lots that includes providing a plurality of operations in the semiconductor manufacturing process, providing a plurality of tools in at least one of the plurality of operations, providing a plurality of yields for each of the plurality of operations, providing a plurality of process paths, calculating an average yield for the plurality of yields, setting the average yield as a response, setting the plurality of operations as control factors, setting the plurality of tools as factor levels in response to at least one of the plurality of operations, determining at least one of the plurality of operations as having the most contribution using an analysis of variance method, wherein the at least one of the plurality of operations causes the responses to change greater than a predetermined level when the plurality of tools are changed, and outputting the at least one of the plurality of operations as the most influential operation.

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L. L. P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000